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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,703	03/19/2004	Jason J. Lin	VIAP0133USA	2702

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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
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EXAMINER
BRINEY III, WALTER F

ART UNIT	PAPER NUMBER
2615	

NOTIFICATION DATE	DELIVERY MODE
07/26/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/708,703	LIN, JASON J.	
	Examiner	Art Unit	
	Walter F. Briney III	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6 and 7* is/are allowed.

6)☒ Claim(s) *1-3,5 and 8-12* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 8, 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Oxford (US Patent 6,405,092 B1).**

Claim 8 is limited to "a method for adjusting the volume of a digital audio signal." The steps of this method are inherently performed by the apparatus set forth in claim 1, the rejection of which is set forth below and incorporated into the rejection of this claim; however, this claim does not require the parallel interface between the FIFO and digital-to-analog processor that claim 1 did, so Oxford alone anticipates all limitations of this method. To facilitate understanding consider the following: the serial receiving step is performed by the serial interface, the setting a loading delay is performed by the volume controller, the parallel forwarding of received bits is performed by the shift register and the processing into an analog audio signal is performed by the digital-to-analog processor. Therefore, Oxford anticipates all limitations of the claim.

Claim 9 is limited to "the method of claim 8," as covered by Oxford. Since the serially received bits of Oxford are received in shift register 360 in a least-significant bit first manner, delaying the loading of bits from register 360 to FIFO 370 right-shifts the bits, thereby attenuating the analog audio signal; this means that shortening the delay

left-shifts the bits, thereby amplifying the analog audio signal. Therefore, Oxford anticipates all limitations of the claim.

Claim 11 is limited to "the method of claim 8," as covered by Oxford. Oxford discloses "attenuating or amplifying the analog audio signal by an amount less than the unit attenuation or amplification resulting from a minimum adjustment of the loading delay." Said attenuating/amplifying is actualized by serial adders 352, 354 and 356—which weight the PCM data, such that the shifting performed in register 360 is less than 6 dB. See column 5, line 59, through column 6, line 7. Therefore, Oxford anticipates all limitations of the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oxford.

Claim 10 is limited to "the method of claim 8," as covered by Oxford. This claim seeks protection similar to what was claimed in claim 9 with the difference that the data modified is received in reverse order (most-significant bit (MSB) first instead of least-significant bit first (LSB)). Oxford, however, states in column 2, lines 25-44, that such an approach would be more conventional than the one taken in his disclosure. Said disclosure suggests that the LSB method is more efficient than the MSB, but fails to

indicate precisely how. Moreover, the applicant is silent regarding any efficiency gains in processing signals in an MSB manner. Common sense dictates that the applicant, thus, has failed to create a new or improved invention in his MSB-based attenuator/amplifier, and the differences are the result of mere design choice.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Oxford to attenuate/amplify signals in scale register 360 in an MSB-manner instead of the disclosed LSB-manner as a matter of design choice.

3. **Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oxford in view of Christopher (US Patent 4,731,851) and further in view of Hasegawa et al. (US Patent 4,931,796).**

Claim 1 is limited to "an audio processing circuit." In rejecting this claim reference is made to US Patent 6,405,092 B1 (herein Oxford). Oxford discloses a method and apparatus for amplifying and attenuating digital audio as set forth in the Abstract. As seen in figure 1, a computer 10 is provided for playing audio over a speaker. See column 3, lines 16-30. The audio playback features are detailed in figures 2 and 3. Figure 3, specifically, is a more detailed version of figure 2, illustrating "a serial interface having an input 310 for receiving a digital audio signal and an output 356/358 for serially outputting bits of the digital audio signal." See column 4, lines 16-20, and column 4, lines 64-67. At the output of the serial interface is "a shift register 360 having a serial input connected to the output of the serial interface for storing bits of the digital audio signal." This register feeds "FIFO buffer 370 having a parallel input

connected to a parallel output of the shift register 360." See column 4, line 64, through column 5, line 13. Lastly, the apparatus for amplifying and attenuating digital audio disclosed by Oxford includes timing & control block 330. This block corresponds to "a volume controller connected to the FIFO by way of signal line 375, and which initiates "loading of bits in the shift register 360 into the FIFO 370 according to a volume control signal 365-375." See column 5, lines 3-57. Nevertheless, Oxford fails to disclose the claimed "digital-to-analog processor connected to a parallel output of the FIFO." Yet, the requirement of reproducing the scaled audio using a loudspeaker itself necessitates the presence of said "digital-to-analog processor;" however, this requirement does not anticipate the claimed arrangement of the processor: "connected to a parallel output of the FIFO." Indeed, the output of FIFO 370 is serial as seen in figure 3. It is respectfully submitted, though, that this parallel connection was obvious to one of ordinary skill in the art at the time of the invention.

The rationale for obviousness in this case rests in the art-recognized suitability and equivalence of both approaches to conveying signals between modules. In particular, both Christopher and Hasegawa teach digital-to-analog signal paths that, without qualification, can be alternately embodied as either serial or parallel datapaths. See both the Abstract of and figure 6 of Christopher as well as column 3, lines 55-59, of Hasegawa.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to embody the serial output of the FIFO 370 with parallel signaling paths as taught by Christopher and Hasegawa because of the art recognized

equivalence between the two signaling schemes. Moreover, parallel interfaces have the potential for increased bandwidth, which will diminish overall processing latency of the audio playback process.

Claim 2 is limited to "the audio processing circuit of claim 1," as covered by Oxford in view of Christopher and further in view of Hasegawa. Since only the presence and orientation of the digital-to-analog processor relative to the FIFO 370 could be reasoned from the disclosure of Oxford, it is required that one of ordinary skill in the art choose or design a suitable processor from knowledge available to that person. One exemplary processor, already discussed supra, is Hasegawa. The Hasegawa conversion circuit has a parallel interface to mate with the parallel obvious parallel output of FIFO 370. In addition, it includes "an analog amplifier 4 connected to an output of the digital-to-analog processor 2." One salient feature of the conversion circuit of Hasegawa is that the converter portion 2 has less inputs than the number of parallel inputs. That is, the m parallel inputs number greater than the n converter inputs. This reduces overall cost, but requires an amplifier 4 to scale the resulting analog output signal. See the Background of the Invention section.

Therefore, it would have been obvious to embody the parallel digital-to-analog processor of Oxford with the processor taught by Hasegawa because one of ordinary skill in the art has no other practical guideline for providing digital-to-analog conversion and because the converter of Hasegawa has a reduced cost over other processors.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oxford in view of Christopher in view of Hasegawa and further in view of Bien (US Patent 6,388,525 B1).

Claim 3 is limited to "the audio processing circuit of claim 2," as covered by Oxford in view of Christopher and further in view of Hasegawa. The variable gain amplifier 4 taught by Hasegawa is of unknown construction and also must be chosen; for example, Bien teaches one type of voltage controlled variable gain amplifier that includes both "a feedback variable resistance Z_f and an input variable resistance Z_S." The benefit to the configuration of Bien is its ability to operate in a linear range over a wide dynamic range, which is ideal for audio generation since non-linear distortion can cause audible artifacts that reduce enjoyment in the case of music or perception in the case of speech—an example of audio reproduction highlighted by Bien's teachings. Further, attenuation does not produce noise. See the Background of the Invention. It follows from the above that the control signal generated by AND gate 9 is also a part of the volume control signal and that said gate is part of the volume controller.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to embody the variable gain amplifier 4 with the amplifier taught by Bien to realize the aforementioned benefits and because one of ordinary skill in the art is practically motivated to choose any prior art solution consistent with audio reproduction.

5. **Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oxford in view of Christopher in view of Hasegawa and further in view of Ledzius et al. (US Patent 5,339,079).**

Claim 5 is limited to "the audio processing circuit of claim 1," as covered by Oxford in view of Christopher and further in view of Hasegawa. It is initially noted that

none of the cited prior art at his point include disclosure, teaching or suggestion to include a mute function. There is, however, no question that the inclusion of mute functions in audio circuits is notoriously well-known, and Official Notice is taken of this fact. Mute circuits, as a review, greatly reduce, or even eliminate, the output of a circuit, such that a rapid decrease in signal level can be attained. The plan obviousness of including a mute signal notwithstanding, one of ordinary skill in the art must still provide logic for implementing the mute function. One particular mute implementation is described by Ledzius in the patent titled: "Digital-to-analog converter with a flexible data interface." Figure 2 illustrates a structure very familiar to that of Oxford, including the input shift register 43 and parallel output register 42, which feeds a digital-to-analog converter including mute circuit 22 as well as blocks 23 through 25, which form the converter kernel. In the event that the mute signal is asserted, complete attenuation, such that all data bits are driven to zero will occur in time increments. See figures 4 and 5 as well as column 4, lines 6-33.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include a mute circuit in the audio circuitry of Oxford as was notoriously well-known to do in the prior art to provide rapid attenuation to a preset level with a single entry by a user.

6. **Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oxford in view of Ledzius.**

Claim 12 is limited to "the method of claim 8," as covered by Oxford. This claim requires "setting each bit of the segment to a predetermined value when the volume

control signal indicates a mute function." This method of muting is obvious for the same reasons set forth in the rejection of claim 5. Therefore, Oxford in view of Ledzius makes obvious all limitations of the claim.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

7. **Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.**

Claim 4 is limited to "the audio processing circuit of claim 3," as covered by Oxford in view of Christopher in view of Hasegawa and further in view of Bien. This claim requires that "the volume controller delays or speeds loading of bits in the shift register into the FIFO...according to...the volume control signal." This occurs in accordance with Oxford's disclosure ranging from column 5, line 3, through column 5, line 57. However, Oxford does not disclose that the volume control signal comprises a coarse component and fine component, where the coarse component controls the delay/speed loading of bits while the fine component controls the variable resistance of the analog amplifier 4 taught by Hasegawa. This is actually contrary to the teachings of the prior art since the amount of volume change effected by buffers 360 and 370 is equal to or less than that generated by amplifier 4. In other words, the control signals of the prior art, at best, are reversed with respect to the claimed volume control signal components. Thus, claim 4 is allowable over the cited prior art.

8. Claims 6 and 7 are allowed.

Claim 6 is limited to "an audio processing circuit." This claim is both independent and recites all the limitations of claims 1 through 4. Thus, claim 6 is allowable over the cited prior art.

Claim 7 depends from claim 6, and is allowable over the cited prior art for at least the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Walter F Briney III
7/23/07